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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/343,872	06/30/1999	TUAN Q. DAO	5201-20400	8423

24319 7590 09/24/2002

LSI Logic Corporation
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EXAMINER

HUYNH, KIM T

ART UNIT

PAPER NUMBER

2181

DATE MAILED: 09/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary

	Application No.	Applicant(s)
	09/343,872	DAO ET AL.
Examiner	Art Unit	
Kim Huynh	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-8 and 10-15 is/are rejected.
- 7) Claim(s) 9 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). _____.
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 6) Other:

DETAILED ACTION

CLAIMS OBJECTION

1. Claim 9 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-8 and 10-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Archer et al. (US 6,148,356)

Archer discloses a data transfer apparatus that comprises:

- A plurality of busses each configured to couple a processing device to a corresponding memory module. (col.2, lines 1-13), (col.5, lines 6-24)

- At least one cross-bus coupled to each of the plurality of busses by one or more bus bridges, wherein the bus bridges each include a set of multiplexers that are configurable to steer signals from the bus to the cross-bus to the bus. (col.2, lines 1-13), (col.4, lines 10-36)
- A memory management unit configured to receive memory access requests from a plurality of processing devices and to responsively configure the bus bridges to steer address and data signals accordingly. (col.2, lines 1-13), (col.4, lines 10-36), (col.5, lines 11-24)
- The memory management unit includes a DMA controller coupled to the cross-bus and configurable to transfer a block of data between said memory modules. (col.7, lines 1-33)
- The memory management unit includes an interrupt controller configurable to assert an interrupt signal to said processing devices after completing a block transfer of data. (col.8, lines 57-65)
- The memory management unit includes one or more request queues, wherein said one or more request queues includes a single transfer queue configured to store access requests relating to single data word transfers. (col.9, lines 1-13)
- One or more request queues includes a block transfer queue configured to store access requests relating to block data transfers. (col.9, lines 1-13)
- One or more request queues includes a message transfer queue configured to store message transfer requests. (col.8, lines 20-35)

- The memory management unit includes an interrupt controller configurable to assert an interrupt signal to a processing device that is an addressee of a message transfer request. (col.8, lines 20-35)
- Port logic connected to the plurality of busses and configured to couple to the processing devices, wherein the port logic is further coupled to the memory management unit and configured to prevent writes to protected memory. (col.5, lines 11-23), (col.6, lines 65-58)
- Plurality of busses includes at least three busses. (see abstract, lines 1-11)
- Processing units providing transfer requests to a memory manager. (col.7, lines 1-63), (col.6, lines 65-67), (col.5, lines 1-23), (col.8, lines 20-35)
- Memory manager setting a router in a conflict-free access pattern in response to said transfer requests, wherein setting said router includes: Memory manager providing control signals to bus bridges that couple local busses between a memory module and a processing device to a cross-bus between the local busses. Processing units accessing memory modules via said router. (col.7, lines 1-63), (col.6, lines 65-67), (col.5, lines 1-23), (col.8, lines 20-35)
- Memory manager determines said conflict-free access pattern in accordance with assigned priorities for each transfer request. (col.8, lines 20-35)

- Memory manager operating a direct memory access (DMA) controller to perform block transfers of data between memory modules. (col.4, lines 8-36)
- Memory manager asserting an interrupt signal to any one of said processor units that is the addressee of a message transfer request (col.8, lines 20-35)
- A high-bandwidth bus (col.4, lines 36-53)

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lange [USPN 6,092,141] discloses selective data read-ahead in bus-to-bus bridge architecture.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Wong can be reached on (703)305-3477 or via e-mail addressed to [Peter.Wong@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7249 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

September 16, 2002

Sumati Lebowitz
SUMATI LEFKOWITZ
PRIMARY EXAMINER